PARALLEL PROCESSING

Quiz No 1

Fill in the Blanks.

1. In the **UMA** system, all processors have equal access time to any memory location.

2. The surge of network capacity tipped the balance from a processor-centric view of computing to a **network**-centric view.

3. Protection is a system feature that prevents processes from making arbitrary access to **resources** belonging to other processes.

4. The data stream is defined as the data traffic exchanged between the **memory** and the processing unit.

5. Parallel computers are either **SIMD** or MIMD.

6. **Distributed** memory is the only way to efficiently increase the number of processors managed by a parallel and distributed system.

7. The SIMD model of parallel computing consists of two parts: a front-end computer of the usual von Neumann style, and a **processor array**.

8. In **wormhole routing**, a packet is divided into smaller units that are called flits (flow control bits) such that flits move in a pipeline fashion.

9. Similar to the NUMA, each processor has part of the shared memory in the **COMA** however, in this case the shared memory consists of cache memory.

10. A shared memory system typically accomplishes **interprocessor** coordination through a global memory shared by all processors.

11. The process of passing bus mastership from one processor to another is called **handshaking**.

12. Programming in the **shared** memory model was easier.

13. In DSM Systems, the hardware architecture follows the **message passing** school of design.

14. **Access control** determines which process accesses are possible to which resources.

15. Processors exchange information through their **interconnection network** in message passing systems.

16. A **cluster** is a collection of stand-alone computers connected using some interconnection network.

17. In the **NUMA** system, each processor has part of the shared memory attached.

18. Parallel processors are computer systems consisting of multiple processing units connected via some **interconnection** network.

19. In the **MISD** category, the same stream of data flows through a linear array of processors executing different instruction streams.

20. In **synchronous** mode of operation, a single global clock is used by all components in the system.

21. **Packet** switching tends to use the network resources more efficiently

22. Communications in **message passing** systems are performed via send and receive operations.

23. The **network latency** is defined as the time to complete a message transfer.

24. In the **circuit** switching mechanism, a complete path has to be established prior to the start of communication between a source and a destination.

25. MIMD parallel architectures fall into two broad categories: **shared memory** or message passing.

26. **Static** networks form all connections when the system is designed rather than when the connection is needed.

27. The **degree** of a network is defined as the maximum number of links (channels) connected to any node in the network.

28. The bus, crossbar, and multistage interconnection topologies are examples of **dynamic** interconnection networks.

29. The multiple bus with **class-based** memory connection has memory modules grouped into classes whereby each class is connected to a specific subset of buses.

30. MIMD Computers with shared memory are known as **tightly** coupled machines.